REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is respectfully requested.

The Examiner objects to the drawings under 37 CFR 1.83(a). The Examiner states that the drawings must show every feature of the invention specified in the claims. The Examiner also requires that the "discharge circuit" recited in claim 12, the "plurality of switches" recited in claim 17 and the "plurality of resistors" recited in claim 20, be shown or the features canceled from the claims.

It is respectfully submitted that a discharge circuit as recited in claim 12 is clearly shown in Fig. 2 when the switch SG is operated according to the timing sequence shown in Fig. 3. Therefore no drawing change is required. With respect to the plurality of switches recited in claim 17, Applicants propose a Fig. 2A in which these switches are shown, in accordance with the description in the specification. The Examiner's approval of this drawing change is respectfully requested.

With respect to the plurality of resistors recited in claim 20, this claim has been canceled without prejudice.

The Examiner objects to claim 12 under 37 CFR 1.75(a) because he wants the term "the voltage source" on line 7 be changed to – said reduced voltage source --. This change has been made except that in place of the word "said" Applicants have used – the --. Similarly with respect to claim 16, Examiner believes that the term "the discharge circuit comprises LEDs of one column of the matrix" should be changed to – said plurality of LEDs is arranged in a column of the matrix --. This change has been made.

The Examiner rejects claims 12-27 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time

the application was filed, had possession of the claimed invention. The Examiner states that the term "a discharge circuit for coupling each of the scan lines to the voltage source at a time when the scan line is not activating a display element" is incorrect. Claim 12 has been amended in order to change the term "the scan line" to – one of the signal lines – in order to correct the claim.

The Examiner states that in addition, in claim 21, the term "a plurality of scan line buffer circuits each coupling a scan line to the reduced voltage source when not driving a display element" is inconsistent with the specification and specifically in figure 5 in the description thereof. The Examiner states that "furthermore, since the buffer circuit is not located between the scan line and the ground potential (i.e., the claimed reduced voltage source), a buffer circuit can't couple a scan line to the reduced voltage source".

This rejection is respectfully traversed. The circuit shown in Fig. 5 specifically shows buffers B0, B1, B2, and B3 connected between a power supply Vss and a reduced voltage supply 32 (Vs). The operation of the buffer circuit is specifically described in the specification at page 8, lines 31-36 in which it states:

"In the interval the pertinent common line CLi is not selected, the control signal SKi is held at the L level and P1 = ON, N1 = OFF, P2 = OFF, N2 = ON, and the positive polarity voltage Vs of the power supply 32 is electrically connected to the common line CLi through the medium of N2. Here, because the voltage Vs of the power supply 32 is set to a level that is considerably lower than the power supply voltage VBB,..." (emphases added).

The Examiner rejects claims 17 and 20 under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Examiner states that with regard to claim 17, the claimed feature "a plurality of switches...source" disclosed in specification at page 7, last paragraph through page 8, line 4 in order to conduct the discharge operation for each common line at their respective individual timing. The Examiner

states that the disclosure does not contain such description and details how the discharge operation for each common line is processed individually during the horizontal scanning period.

This rejection is respectfully traversed. There is no limitation in claim 17 that each of the scan lines is individually discharged. There is no reason why these switches could be operated in the same way as switch SG shown in Fig. 2. Since the claim does not require the feature that the Examiner states is not properly described, Applicants believe that the '112, first paragraph rejection must fail.

With respect to claim 20, this claim has been canceled without prejudice.

The Examiner rejects claim 12-27 under 35 U.S.C. 102(a) as being anticipated by Applicant's Admitted Prior Art (AAPA). The Examiner states that noting in figures 7-8 and the corresponding description, the claimed invention is read by AAPA because it discloses a LED dot matrix display comprising a circuit to reduce erroneous activation of the display element and herein the Examiner recites LEDs $_{00-30}$ a switch F_0 a current source J_0 and ground potential. The Examiner states that the elements of the claims are read in the reference.

This rejection is respectfully traversed. In order for a '102 rejection to apply it is necessary that all the elements in the claim be found in the reference. While it is clear that the reference shows a scanning LED display, it is also clear that the present invention contains a discharge circuit whereas the prior art is clearly described as not having a discharge circuit. The circuit comprising LEDs $_{00-30}$ as switch F_0 is one of the scan lines in the display. As such, it does not couple the scan line to a reduced voltage source at a time when one of the signal lines is not activating all the display elements. In effect, the switch at 0 is used to activate the LEDs switches connected a part of display. The key here is to operate the switch SG in Fig. 2 according to the timing diagram shown in Fig. 3. This is not shown or suggested in the prior art but it is described clearly in claim 12. Accordingly, claim 12 is clearly distinguished from this

reference and is not anticipated by or rendered obvious by the reference. Claims 13-27 are dependent either directly or indirectly on claim 12, and are therefore patentable for the same reason.

Accordingly, Applicants believe the application as amended, is in condition for allowance, as such action is respectfully requested.

Respectfully submitted,

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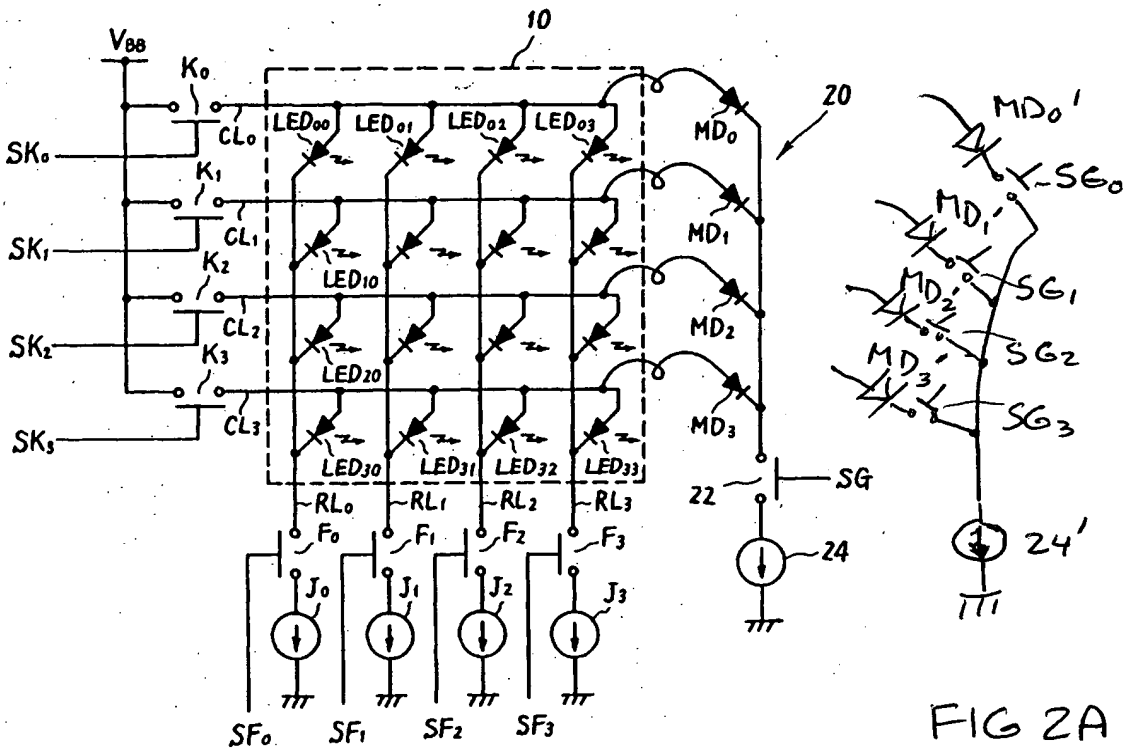

FIG 2A

FIG. 2

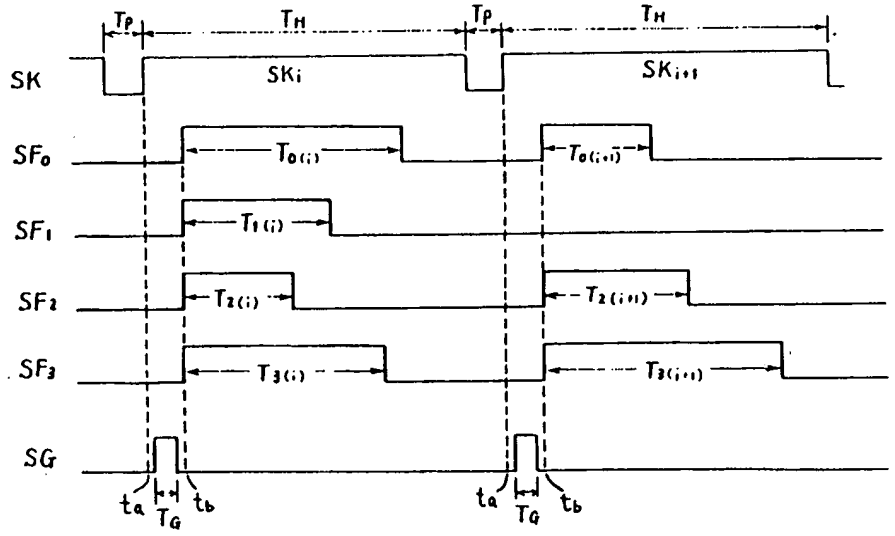

FIG. 3